That which is claimed:

1. A method for testing a field programmable gate array comprising:

(a) applying a test pattern approximately simultaneously to a first path under test in the field-programmable gate array and a second path under test in the field-programmable gate array, wherein the first path under test and the second path under test have substantially the same propagation delays in a fault free circuit;

(b) receiving a first output signal indicating that the test pattern has propagated through at least one of the first path under test and the second path under test;

(c) receiving a second output signal that indicates the test pattern has propagated through each of the first path under test and the second path under test;

(d) determining the interval between receiving the first output signal and the second output signal; and

(e) identifying a fault in at least one of the first path under test and the second path under test when the interval exceeds a threshold.

2. The method of claim 1, wherein the determining the interval between the first output signal and the second output signal comprises:

activating an oscillating signal after receiving the first output signal;

deactivating the oscillating signal after receiving the second output signal; and

counting the number of oscillation cycles occurring while the oscillating signal is active.

3. The method of claim 1, wherein the test pattern comprises a high-to-low transition.

4. The method of claim 1, wherein the test pattern comprises a low-to-high transition.

5. The method of claim 1, further comprising before step (a) generating the test pattern.

6. The method of claim 1, further comprising before step (a) configuring the first path under test and the second path under test.

7. The method of claim 1, further comprising before step (a) developing a configuration for the first path under test and the second path under test.

8. The method of claim 1, wherein:

the first path under test comprises a fast path; and

the second path comprises a slow path.

9. The method of claim 1, wherein at least one of the first path under test and the second path under test comprises at least one programmable logic block (PLB) configured as an adder for computing the k-bit sum (S) of two k-bit inputs, A and B, and having a carry-in (Cin) and carry-out (Cout).

10. The method of claim 9, wherein:

applying the test pattern comprises applying a raising transition at Cin and B and a 0 vector at A; and

receiving the first and second output signals comprises receiving raising transition at Cout.

11. The method of claim 9, wherein:

applying the test pattern comprises applying a falling transition at Cin and B and a 1 vector at A; and

receiving the first and second signals comprises receiving a falling transition at Cout.

12. The method of claim 9, wherein:

applying the test pattern comprises applying a raising transition at Cin, a 0 vector at A, and a 1 vector at B; and

receiving the first and second signals comprises receiving a falling transition at S.

13. A system for testing a field programmable gate array comprising:

an input;

a first path under test in the field-programmable gate array, the first path under test in communication with the input;

a second path under test in the field-programmable gate array, the second path in communication with the input, wherein the second path has an expected propagation delay substantially the same as the first path under test; and

an output response analyzer in communication with the first path and the second path and operable to determine an interval between the time a data signal propagates through the first path under test and the second path under test.

14. The system of claim 13, wherein the output response analyzer comprises:
an oscillator; and
a counter in communication with the oscillator.

15. The system of claim 14, wherein the oscillator comprises:
an NAND gate in communication with the first path under test;
a first OR gate in communication with the second path under test; and
a second OR gate in communication with the NAND gate and the first OR gate.

16. The system of claim 14, wherein the oscillator comprises:
an OR gate in communication with the first path under test;
a first NAND gate in communication with the second path under test; and
a second NAND gate in communication with the OR gate and the first NAND gate.

17. The system of claim 13, wherein the programmable logic blocks in the first path under test and the second path under test comprise identity functions.

18. The system of claim 13, wherein each of the first path under test and the second path under test comprises at least one lookup table (LUT) and where each LUT is configured to produce a transition when the input of the LUT changes to a specified target address.

19. The system of claim 18, wherein the LUT contents of the target address comprises a 1 and the LUT contents of all other addresses comprise a 0.

20. The system of claim 18, wherein the LUT contents of the target address comprises a 0 and the LUT contents of the all other addresses comprise a 1.

21. The system of claim 18, wherein neither of the first path under test and the second path under test comprises a flip-flop.

22. The system of claim 21, wherein each LUT comprises k inputs and each of the first path under test and second path under test comprises consecutive groups of 2^k pairs of LUT's, wherein each of the groups comprises the same configuration and each pair comprises a different target address.

23. The system of claim 13, wherein each of the first path under test and the second path under test comprises:

a first programmable logic block configured as an adder for computing the k-bit sum (S) of two k-bit inputs, A and B, and having a carry-in (Cin) and carry-out (Cout).

24. The system of claim 23, wherein the output response analyzer is connected to the Cout output.

25. The system of claim 23, further comprising a second programmable logic block configured identically to the first programmable logic block, wherein the Cin input of the second programmable logic block is connected to the B and Cout outputs of the first programmable logic block.

26. The system of claim 23, wherein the output response analyzer is connected to the S output.

27. The system of claim 23, further comprising a second programmable logic block configured identically to the first programmable logic block, wherein the A input of the second programmable logic block is connected to the S output of the first programmable logic block.

28. The system of claim 23, further comprising:

a third programmable logic block configured identically to the first programmable logic block, wherein the Cin input of the third programmable logic block is connected to the Cout output of the second programmable logic block; and

a fourth programmable logic block configured identically to the first programmable logic block, wherein the A input of the third programmable logic block is connected to the S output of the third programmable logic block

29. The system of claim 23, further comprising:

a second programmable logic block configured identically to the first programmable logic block, wherein the Cin input of the second programmable logic block is connected to the Cout output of the first programmable logic block;

a third programmable logic block configured identically to the first programmable logic block, wherein the A input of the third programmable logic block is connected to the S output of the second programmable logic block; and

a fourth programmable logic block configured identically to the first programmable logic block, wherein the Cin input of the fourth programmable logic block is connected to the Cout output of the third programmable logic block

30. The system of claim 13, wherein the paths under test, the test pattern generator, and the output response analyzer are all contained in the same vertical self-testing area (V-STAR).

31. The system of claim 13, wherein the paths under test, the test pattern generator, and the output response analyzer are all contained in the same horizontal self-testing area (H-STAR).

32. The system of claim 13, wherein each path under test comprises a horizontal segments contained in a H-STAR and a vertical segment contained in a V-STAR, and further comprising a configurable interconnect point configured at the intersection of the V-STAR and the H-STAR connecting the said horizontal and vertical segments.

33. The system of claim 32, wherein the test pattern generator drives the horizontal segment and the output response analyzer observes the vertical segment of the paths under test.

34. A system for delay-fault testing of an FPGA, wherein the FPGA under test comprises a plurality of parallel vertical self-testing areas (V-STAR's), and each V-STAR comprises the delay-fault testing system of claim 13.

35. A system for delay-fault testing of an FPGA, wherein the FPGA under test comprises a plurality of parallel vertical self-testing areas (H-STAR's), and each H-STAR comprises the delay-fault testing system of claim 13.

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